REMARKS

Reconsideration and allowance are respectfully requested. No new matter is added by this Amendment.

Of the pending claims, claims 1-10 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,574,388 to Barbier, et al. ("Barbier"). Applicant respectfully traverses this rejection in view of the amendments and remarks herein.

Independent Claim 1

Independent claim 1 as amended recites a first reconfigurable interconnect stage, a second reconfigurable interconnect stage having outputs coupled to inputs of the first reconfigurable interconnect stage via feedback paths, and a third reconfigurable interconnect stage. Claim 1 further recites that each of the feedback paths couples one of the outputs of the second reconfigurable interconnect stage to one of the inputs of the first reconfigurable interconnect stage without passing through the third reconfigurable interconnect stage. An illustrative embodiment consistent with claim 1 is shown in Figs. 8 and 9 of Applicant's specification.

The Office action attempts to compare the first reconfigurable interconnect stage with element 104 of Barbier, the second reconfigurable interconnect stage with element 114b of Barbier, and the third reconfigurable interconnect stage with element 622 of Barbier.

As can be seen, Barbier does not teach or suggest the recited feedback path from the second reconfigurable stage to the first reconfigurable stage without passing through the third reconfigurable stage. Rather, the outputs of element 114b must first pass through element 622 of Barbier before feeding back to element 104 (via I/O pins 113 and 114a).

The Examiner appears to believe that I/O pins 113 allow communication directly from element 114b to element 114a (see Office Action, p. 4). In particular, the Examiner argues that element 113 is a bridge rather than an in/out switch. Applicant respectfully disagrees; element 113 is explicitly referred to in Barbier as I/O (input/output) pins, *not* as a bridge.

Fig. 3 of Barbier represents a single FPGA. The FPGA has input and output physical pins, that is, I/O pins 113, just like any other integrated circuit. The sole disclosed purpose of I/O pins

113 is to provide inputs/outputs to/from FPGA 100. (Barbier, col. 4, lines 35-36). Each of I/O pins 113 can be statically configured to be either an input or an output pin. (Barbier, col. 4, lines 36-38). However, nowhere does Barber explicitly or implicitly indicate that elements within the same FPGA can communicate with each other via FPGA I/O pins 113. Nor is such communication inherent/required.

Accordingly, Barbier does not teach or suggest a feedback path from the second reconfigurable interconnect stage to the first reconfigurable interconnect stage without passing through the third reconfigurable interconnect stage, as claimed.

For at least these reasons, it is submitted that claim 1 is allowable over Barbier.

Independent Claims 4, 6, and 8

It is submitted that claims 4, 6, and 8 are also allowable over Barbier for at least similar reasons as those discussed above with regard to claim 1.

Dependent Claims

The dependent claims are also allowable by virtue of depending from allowable independent claims, and further in view of the additional features recited therein.

Conclusion

All rejections having been addressed, it is submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested. Should the Examiner have any questions, the Examiner is invited to contact the undersigned at the number below.

Respectfully submitted,

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